

Figure 1

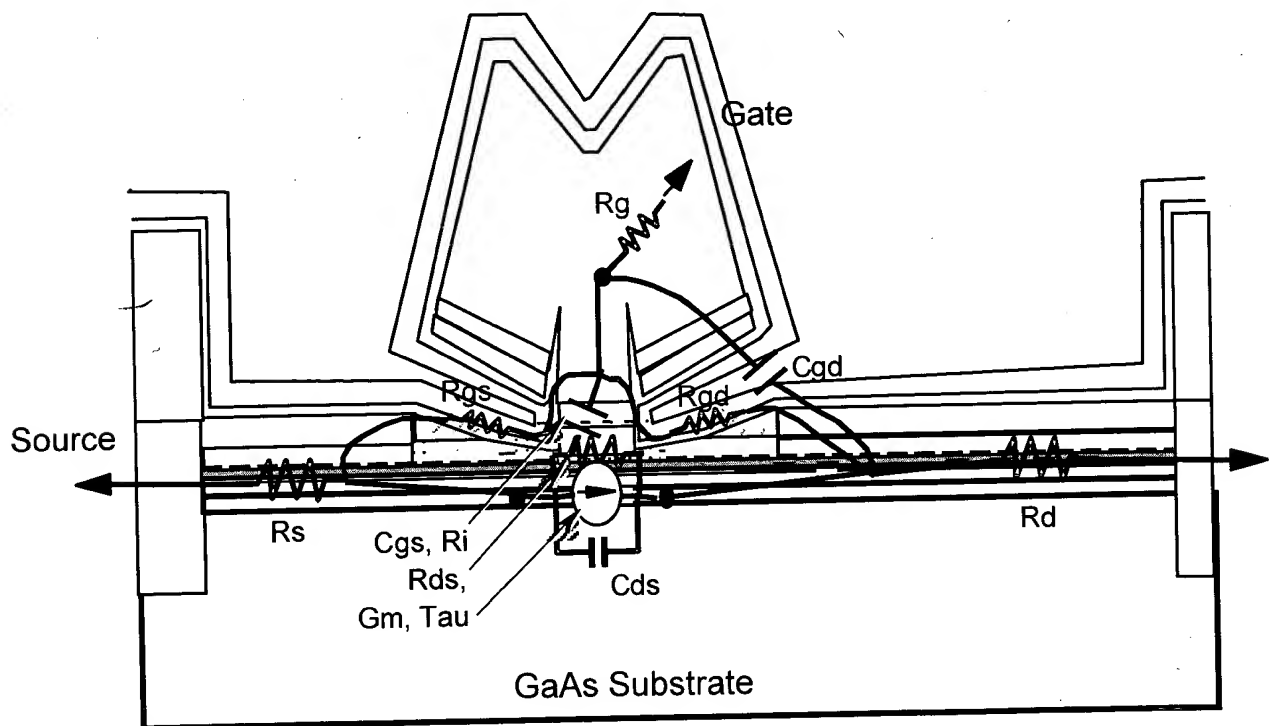


Figure 2

00904860

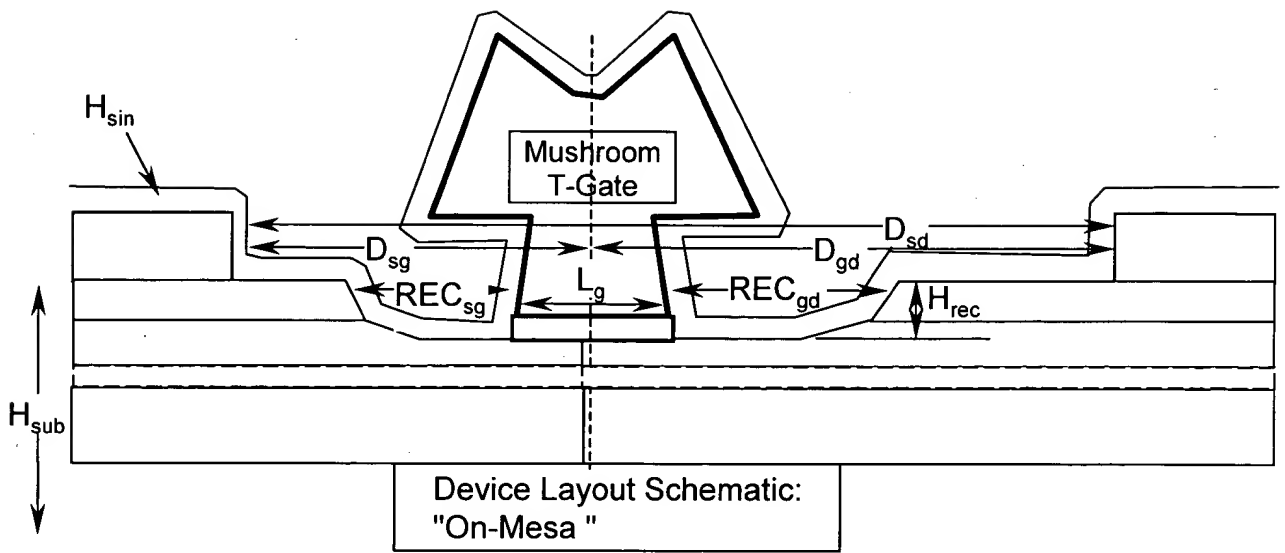


Figure 3

Single Recess Geometry

The schematic diagram shows a cross-section of a device with a central gate region. The gate is recessed into the substrate, with a recess depth d and a recess angle a . The gate length is L_g and the gate position is x_g . The source and drain regions are separated by a distance w_d and have widths w_s and w_d respectively. The substrate thickness is H_{sub} .

Ohmic Contacts		Recess Geometry	
Separation / μm	w_d 2	Width / μm	w .52
Source width / μm	w_s 10	Position / μm	x .8
Drain width / μm	w_d 10	Depth / μm	d .77E-01
		Angle / degrees	a 60
Schottky Contact		Inter-electrode Capacitances / fF	
Gate length / μm	L_g .15	C_{gs} 8.6	C_{gd} 8.1
Gate position / μm	x_g .8	E_{dsp} 43	<input type="checkbox"/> Auto

OK Reset Cancel

Figure 4

HEMT Active Layer

Layer 10

Layer 9

Layer 8

Layer 7

Layer 6

Layer 5

Layer 4

Layer 3

Layer 2

Layer 1

Buffer

Substrate

GaAs		Nd	6.00E18	500Å
AlGaAs	25%	Na	1.00E14	480Å
AlGaAs	25%	Nd	2.00E19	20Å
AlGaAs	25%	Na	1.00E14	20Å
InGaAs	22%	Na	1.00E14	140Å
AlGaAs	25%	Na	1.00E14	30Å
AlGaAs	25%	Nd	6.00E18	16Å
AlGaAs	25%	Na	1.00E14	300Å
AlGaAs	16.5%	Na	1.00E14	150Å
AlGaAs	8.5%	Na	1.00E14	150Å
GaAs				3000Å
S.I. GaAs Substrate				

Edit Layers

Add

Delete

Insert

Move

Copy

Reset

OK

Cancel

NEW Device Layer

Layer no	td	Ma
1	0.0010	SiO2
2	0.0010	SiO2
3	0.0010	SiO2
4	0.0010	SiO2
5	0.0010	SiO2
6	0.0010	SiO2
7	0.0010	SiO2
8	0.0010	SiO2
9	0.0010	SiO2
10	0.0010	SiO2

td: Thickness
Ma: Material

3.1. GaAs Substrate

GaAs Substrate

Figure 6

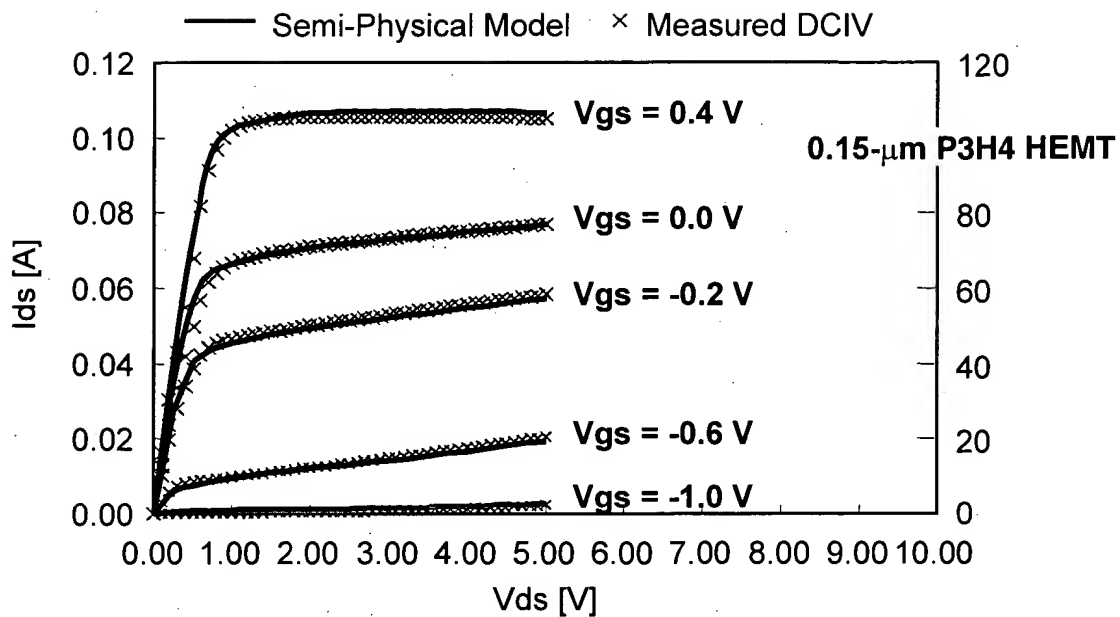


Figure 7

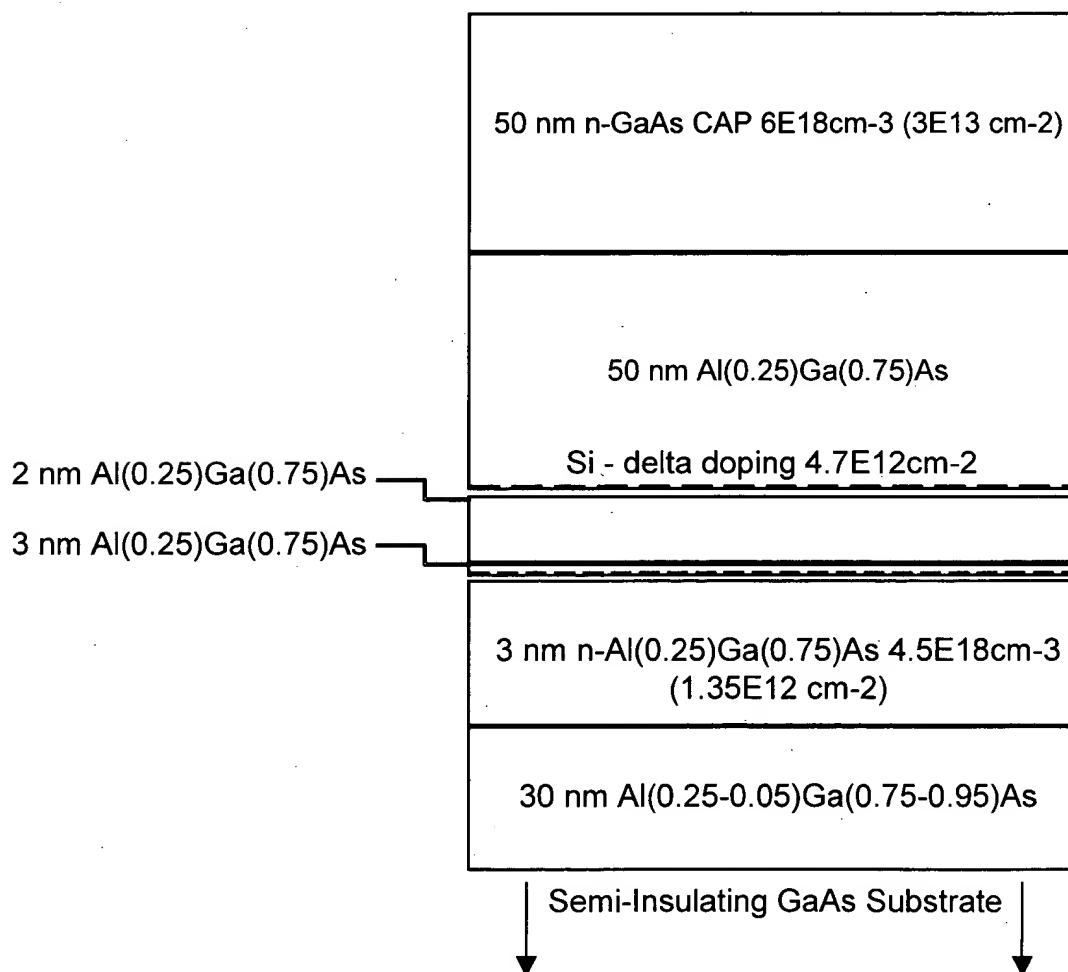


Figure 8

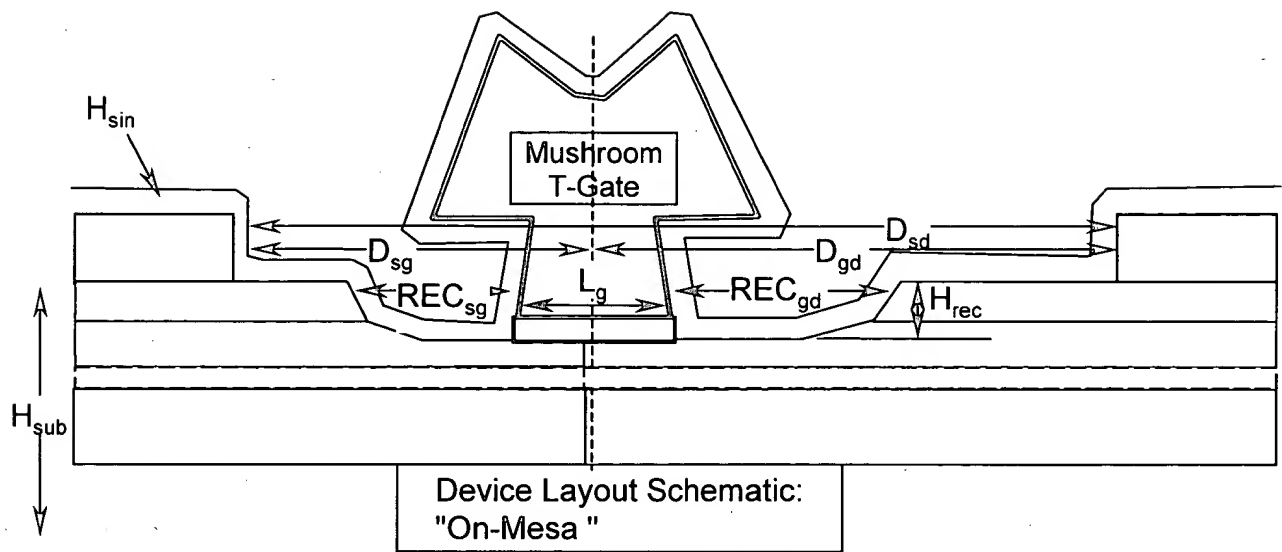


Figure 9

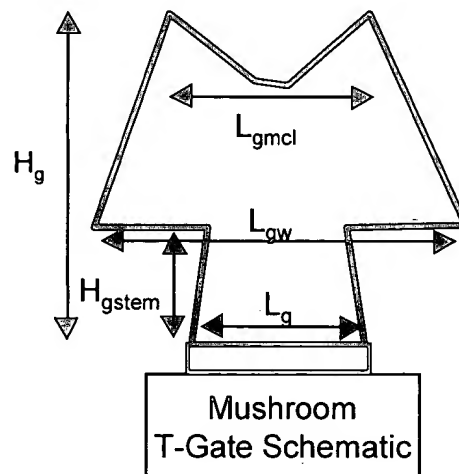


Figure 10

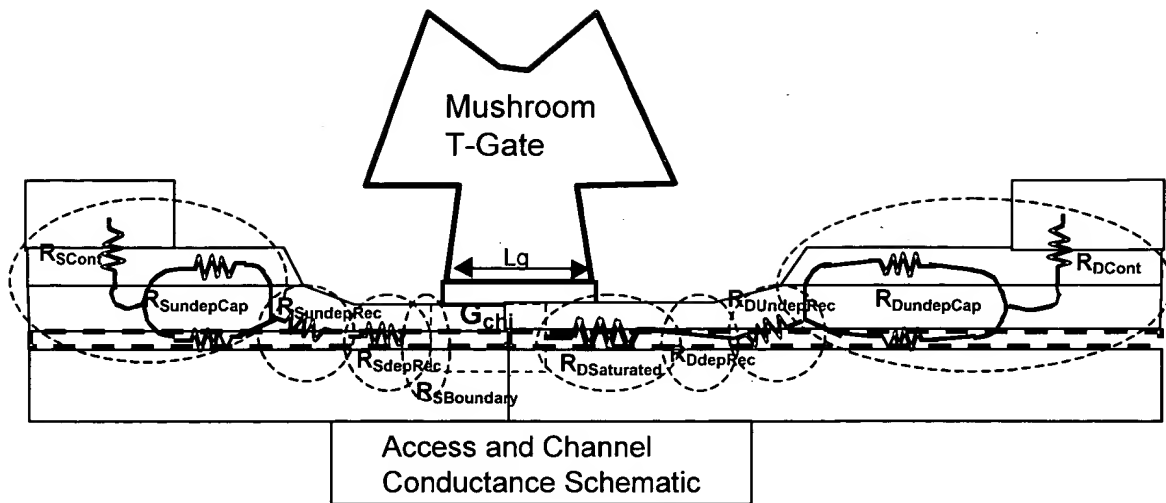
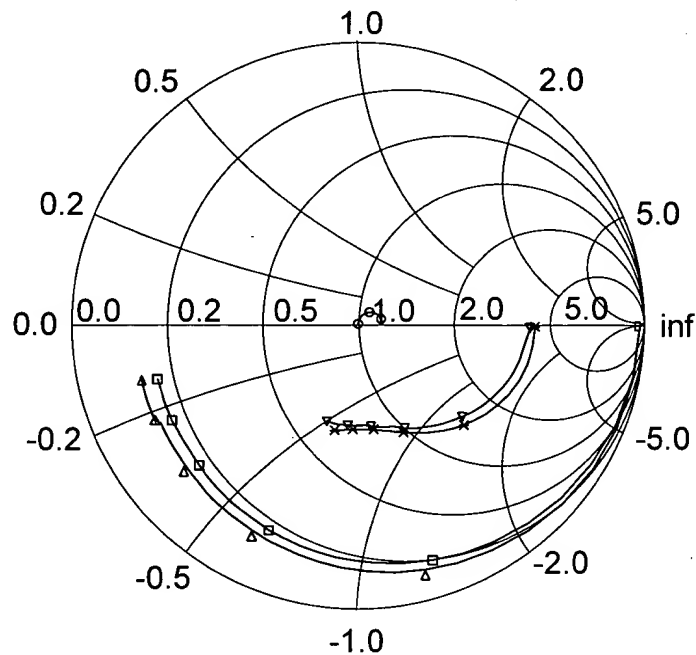


Figure 11

□ measure SMAT1 meas_4200AB_2vidpk-GTPA4 S[1,1]
 ○ measure SMAT1 meas_4200AB_2vidpk-GTPA4 S[1,2]
 ▽ measure SMAT1 meas_4200AB_2vidpk-GTPA4 S[2,2]
 △ Simulated SMAT1 cp100-semiphys S[1,1]
 ◇ Simulated SMAT1 cp100-semiphys S[1,2]
 × Simulated SMAT1 cp100-semiphys S[2,2]

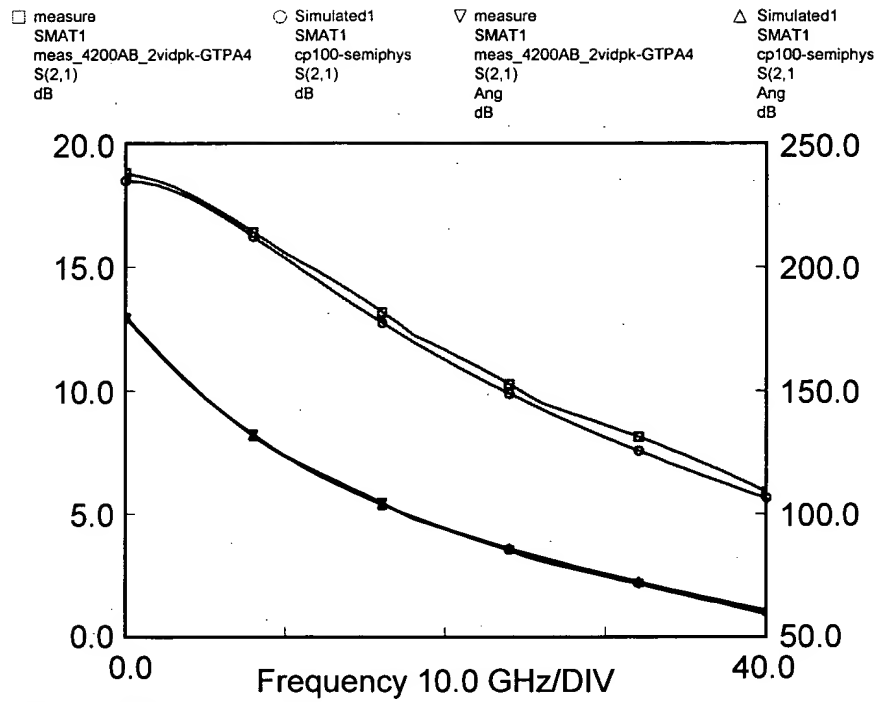


Frequency 0.05 to 40.05 GHz

Measured vs Modeled S-parameters
 Simulated Equivalent Circuit Element Values
 via Semi-Physical HEMT Model

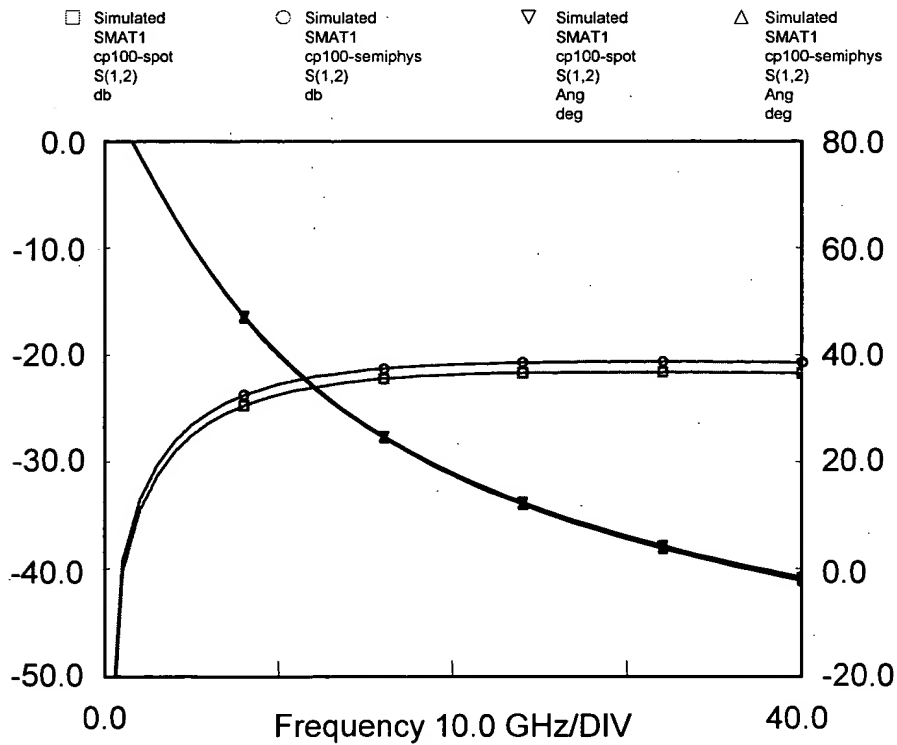
Figure 12

FOE240" 00504860



Measured vs Modeled S12
Simulated Equivalent Circuit Element Values via
Semi-Physical HEMT Model

Figure 13



Measured vs Modeled S12
Simulated Equivalent Circuit Element Values via
Semi-Physical HEMT Model

Figur 14

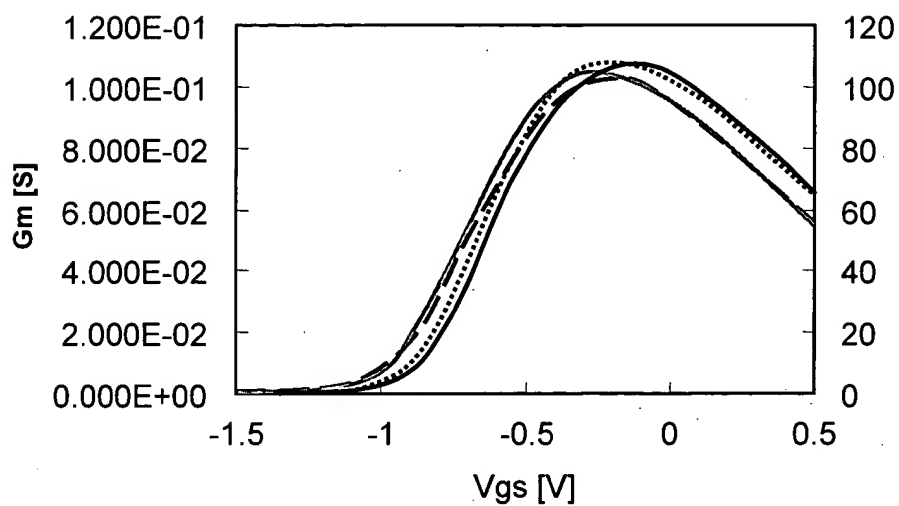


Figure 15

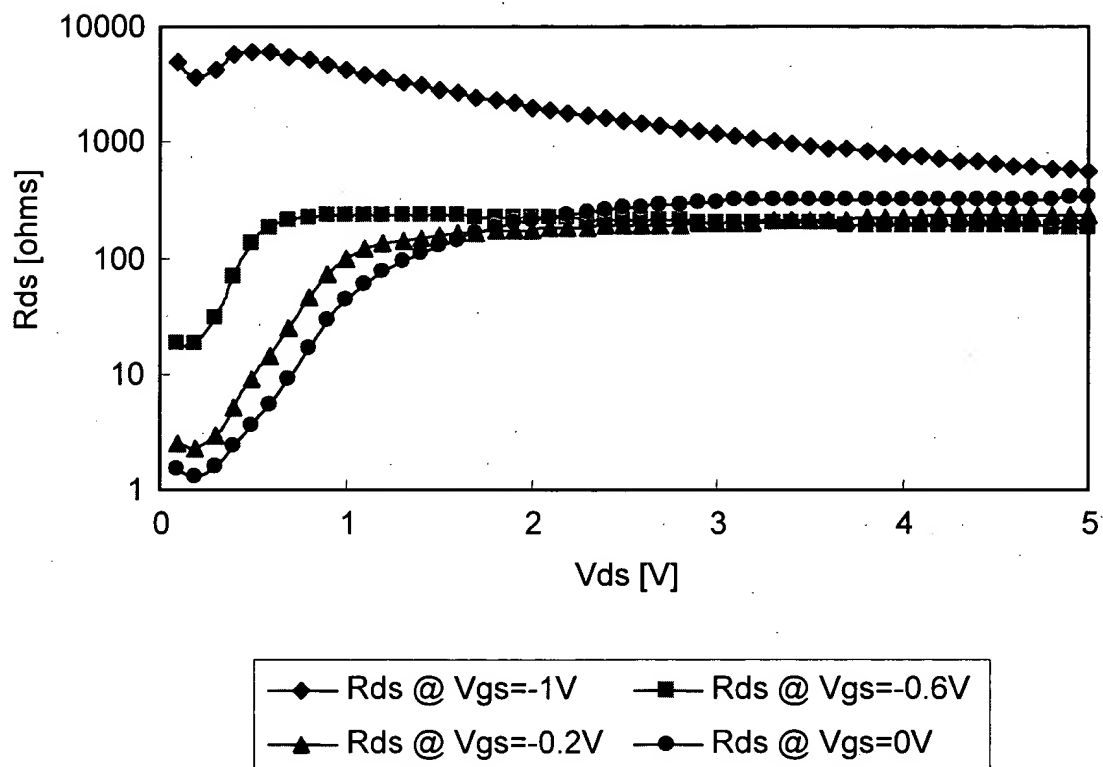


Figure 16

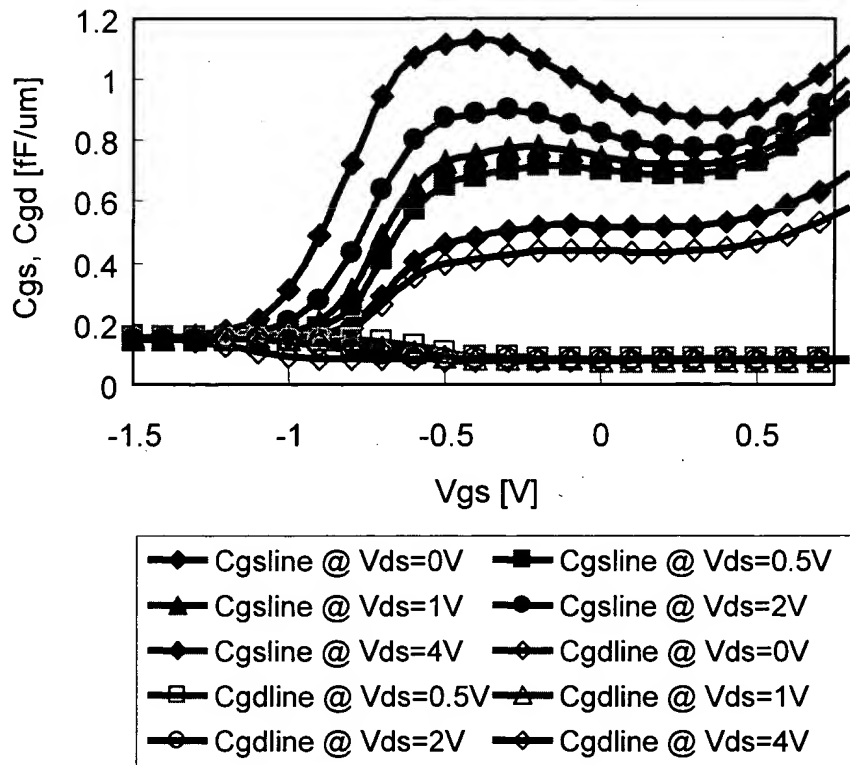


Figure 17

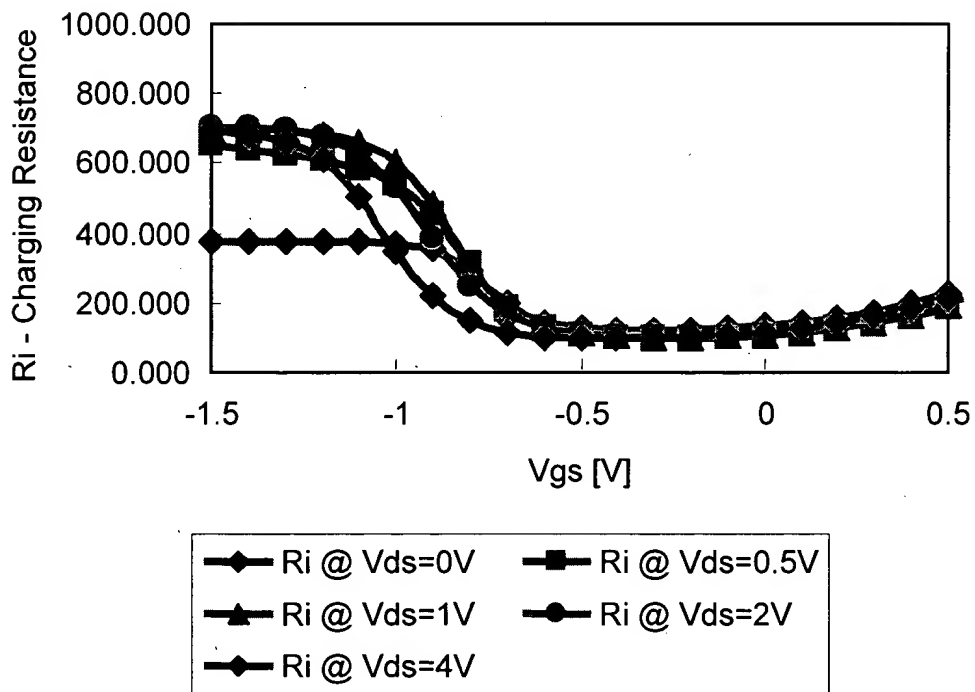


Figure 18

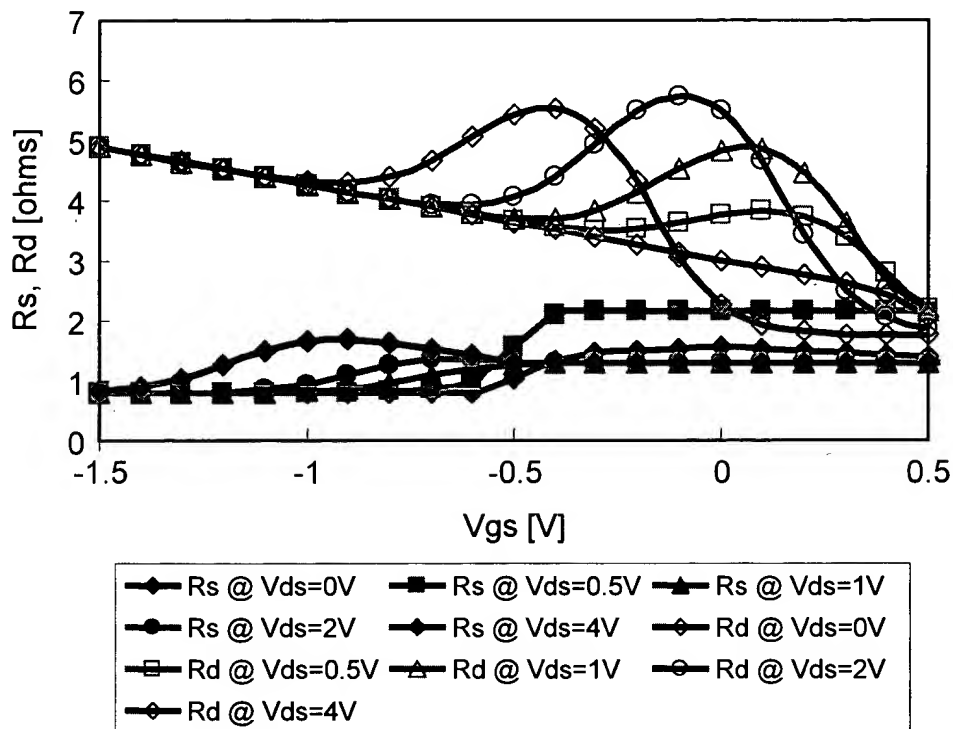


Figure 19

Measured vs Simulated Bias- Dependent Gain @ 23.5 GHz

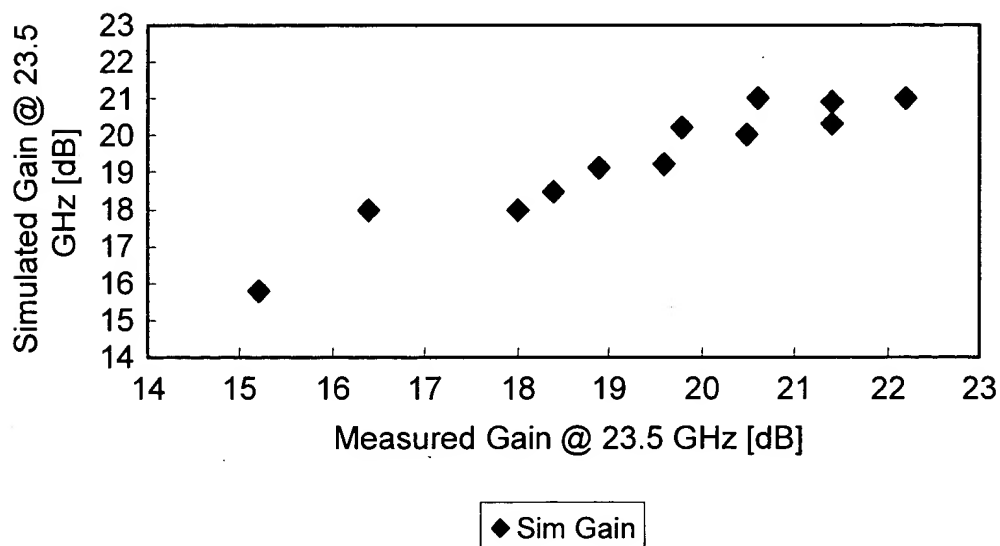


Figure 20

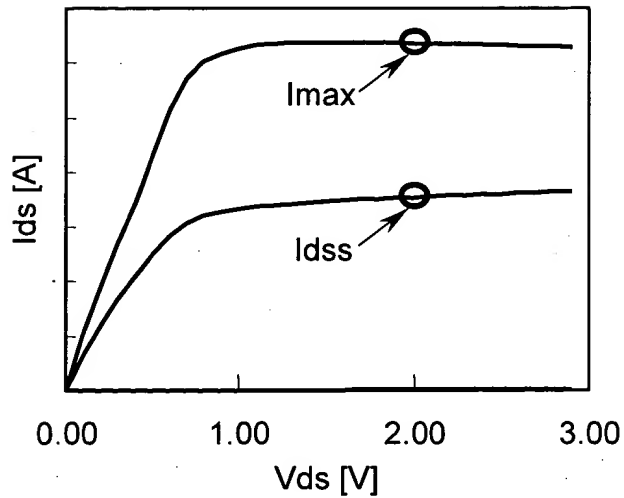


Figure 21A

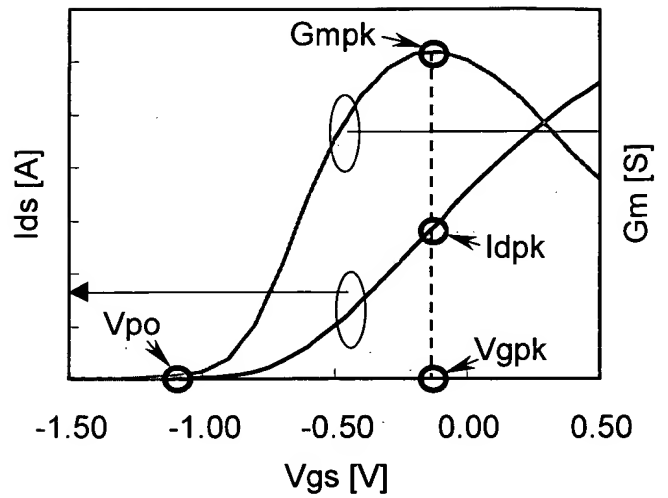


Figure 21B

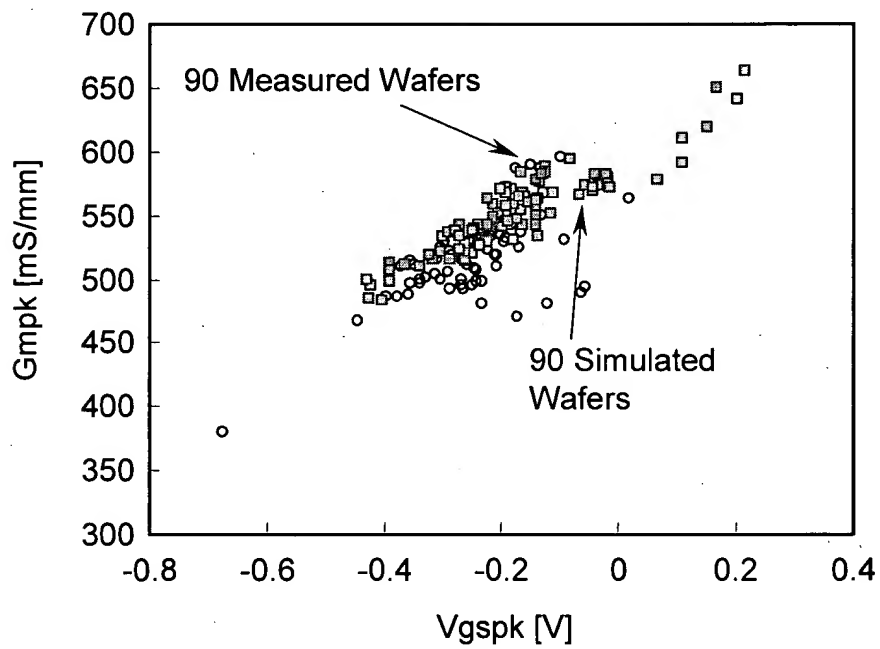


Figure 22

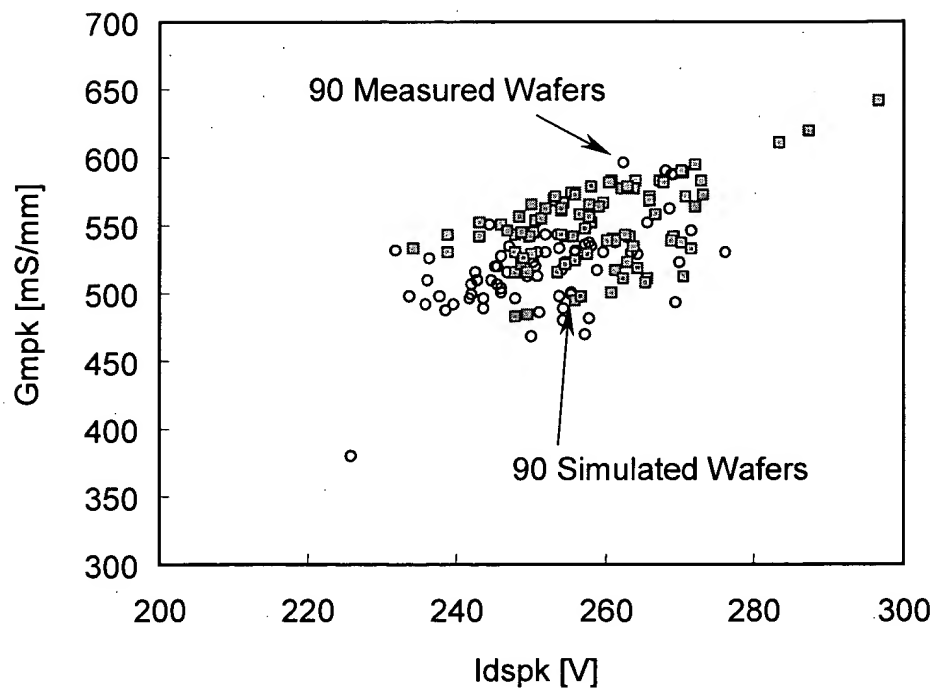


Figure 23

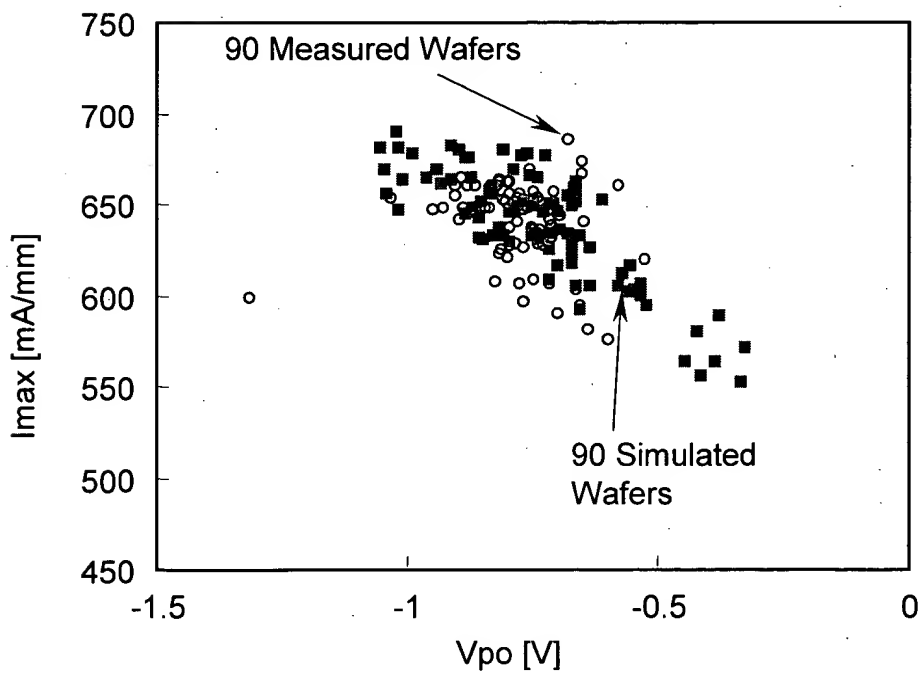


Figure 24

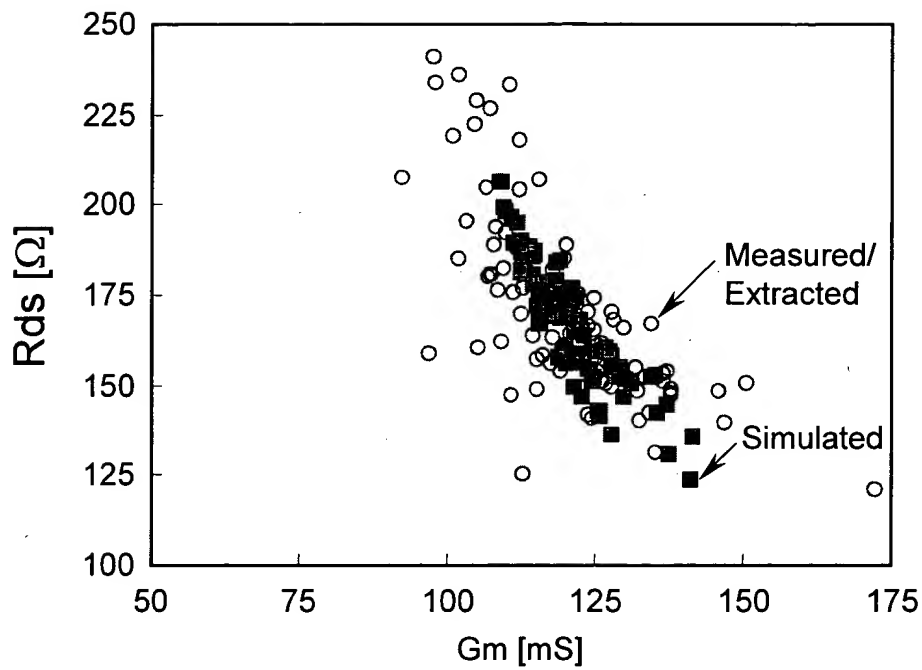


Figure 25

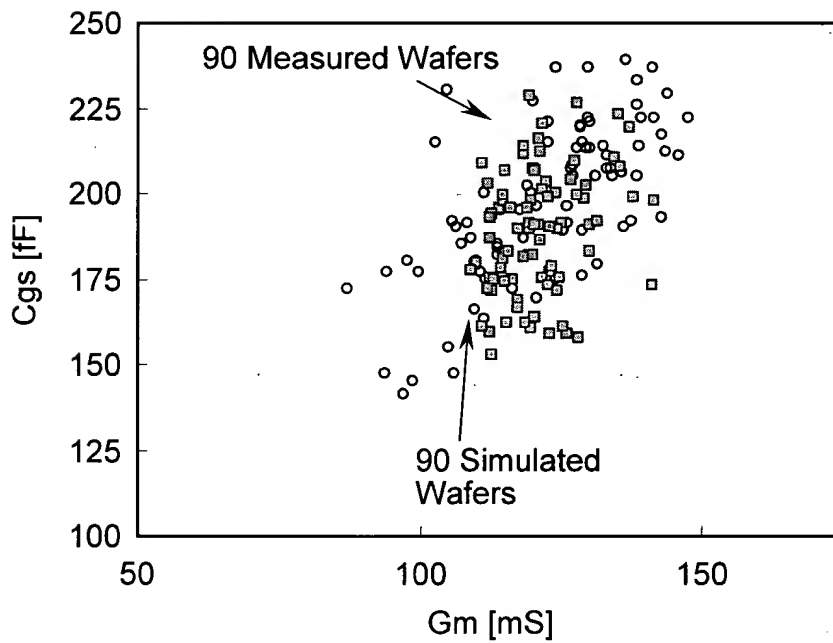


Figure 26

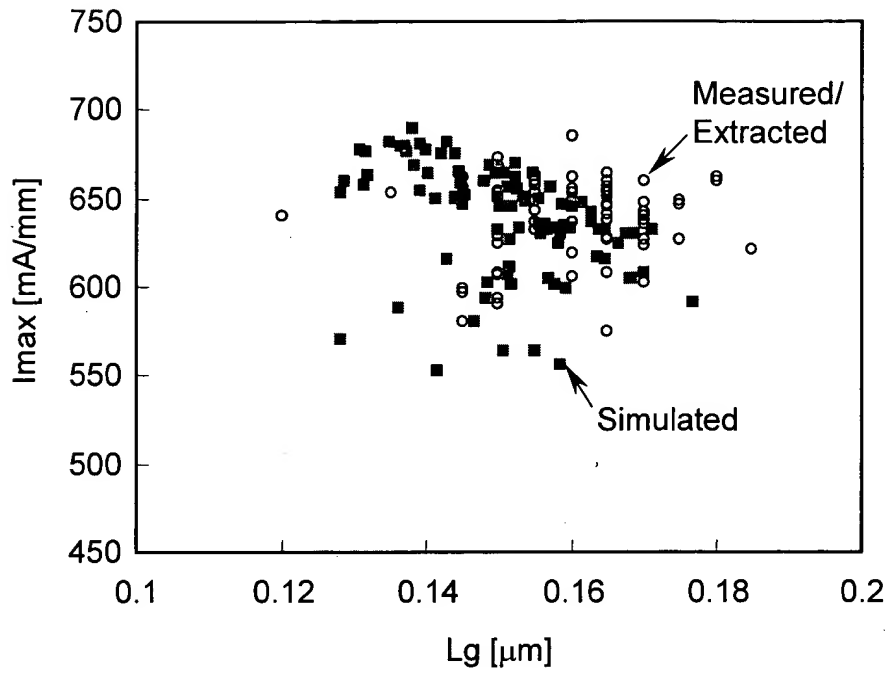


Figure 27

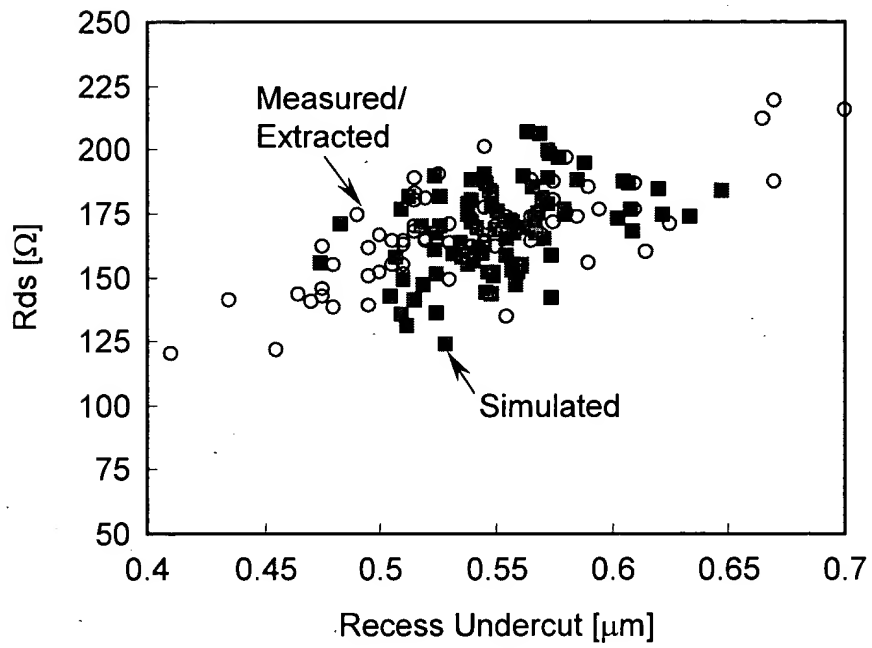


Figure 28